Multiplexer and De-Multiplexer

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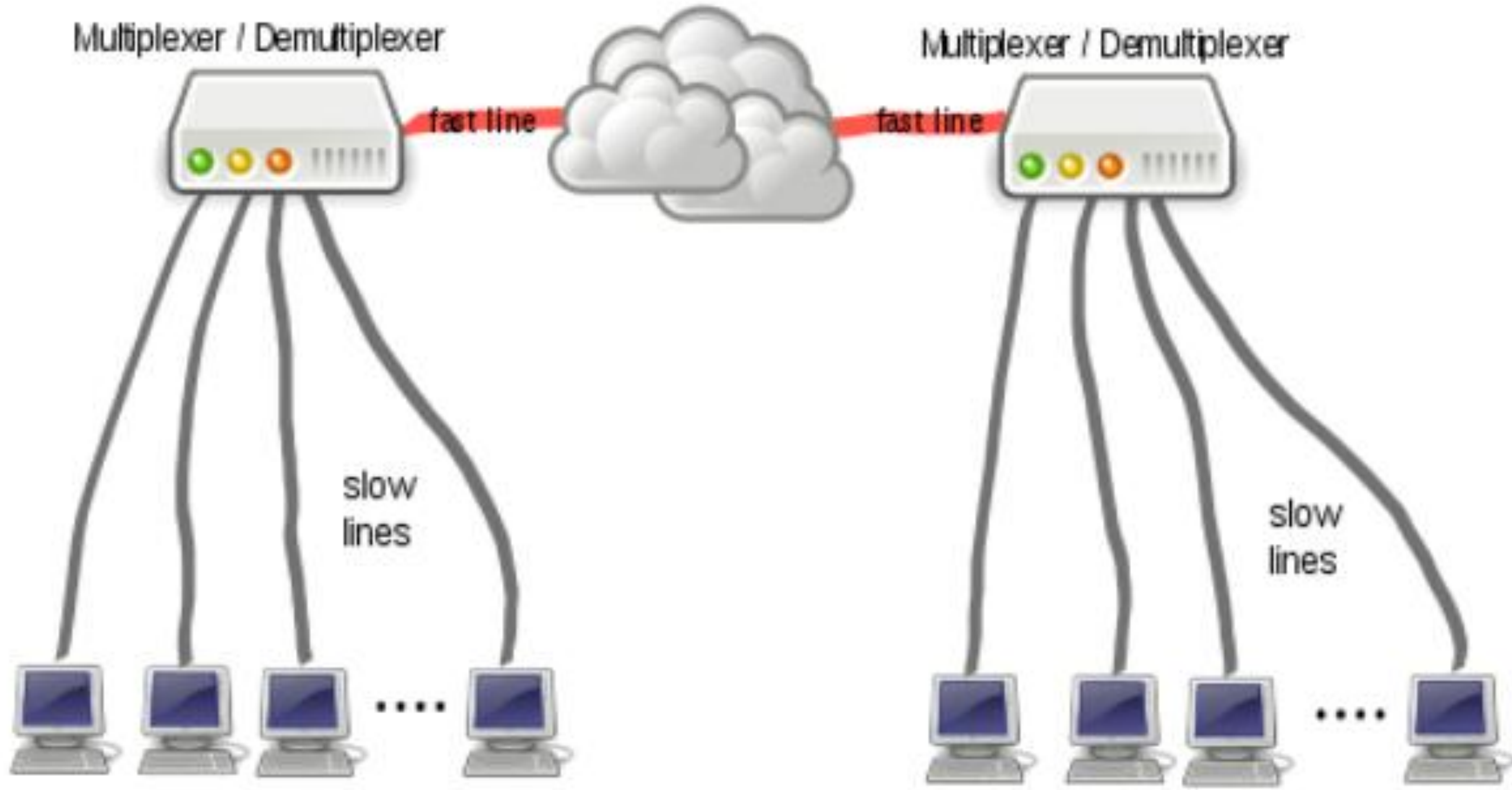
Data Selection Function

- Two types of circuits that select data are the Multiplexer and the Demultiplexer.
- Multiplexer (MUX), switches digital data from several input lines onto a single output line in a specified time sequence.
- Multiplexer (MUX) can be represented by an electronic switch operation that sequentially connects each of the input lines to the output line.

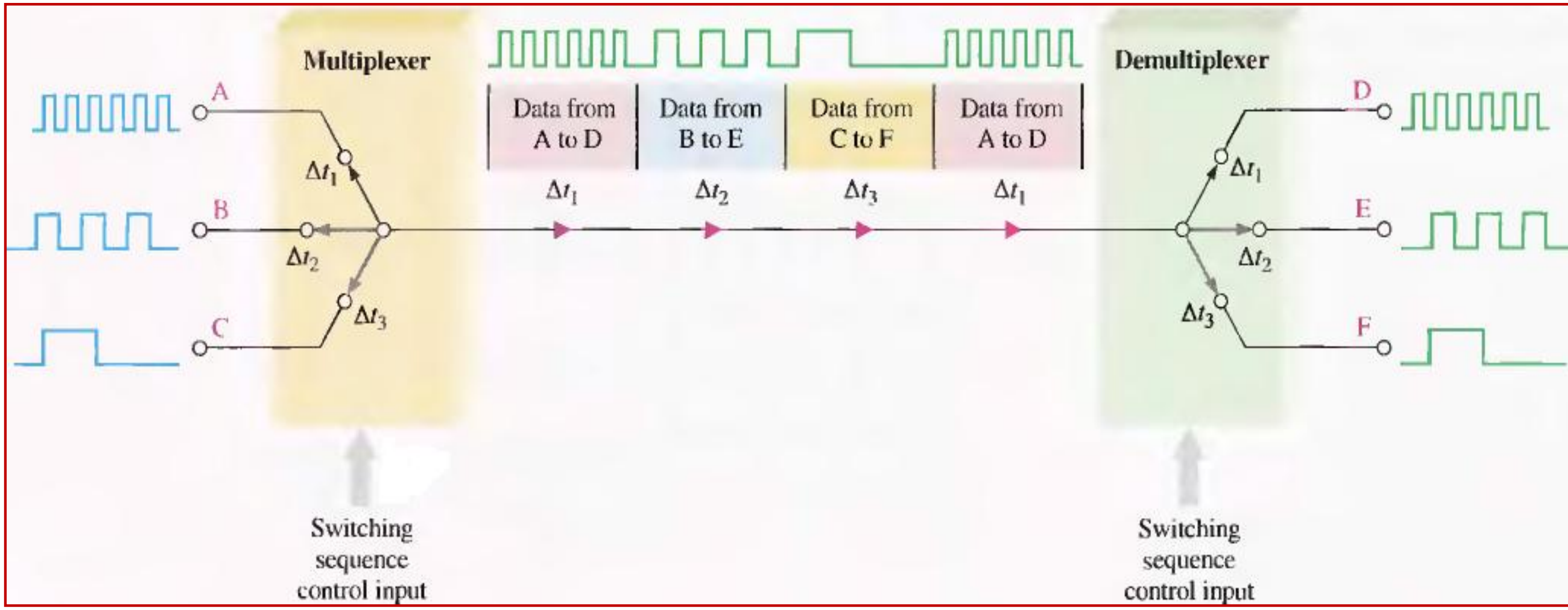
MUX and DeMUX

- The Demultiplexer (Demux) is a logic circuit that switches digital data from one input line to several output lines in a specified time sequence.
- Multiplexing and De-Multiplexing are used when data from several sources are to be transmitted over one line to a distant location and redistributed to several destinations.

MUX and DeMUX



MUX and De-MUX

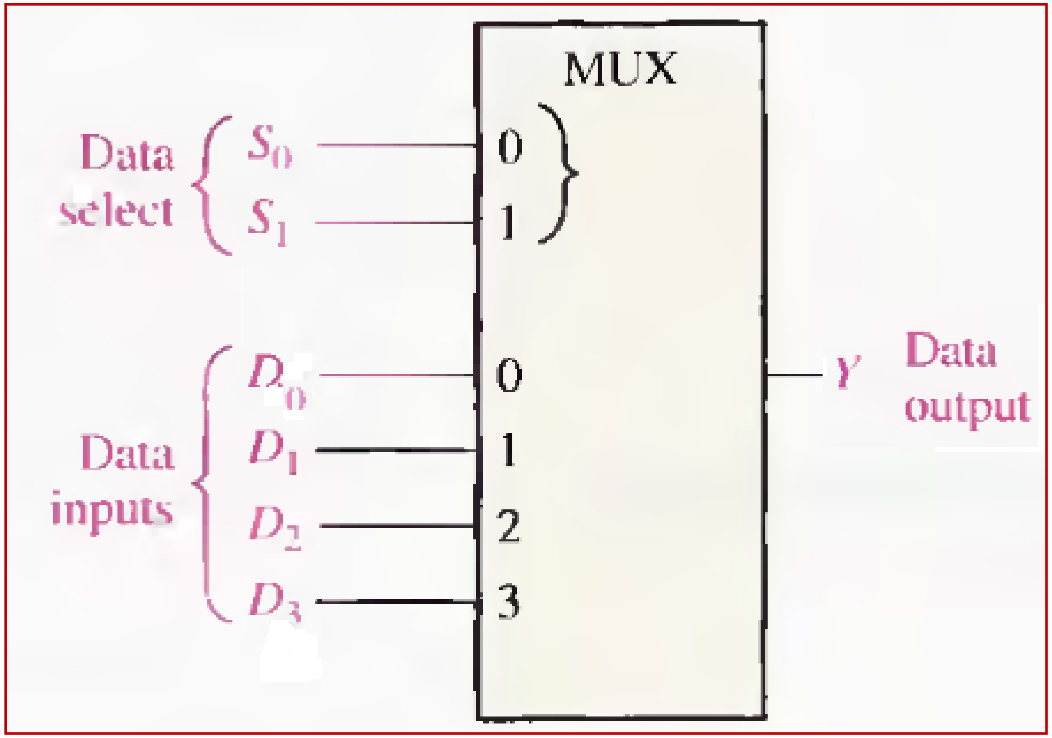


Multiplexer

- A Multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination.
- The basic multiplexer has several data-input lines and a single output line.
- It also has data-select inputs. which permit digital data on anyone of the inputs to be switched to the output line.
  - Multiplexers are also known as data selectors.

Multiplexer

- A logic symbol for a 4-input multiplexer (MUX) is shown in Figure,



Multiplexer

- there are two data-select lines because with two select bits. anyone of the four data-input
- lines can be selected.

DATA-SELECT INPUTS		INPUT SELECTED
S_1	S_0	
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Logic Circuitry

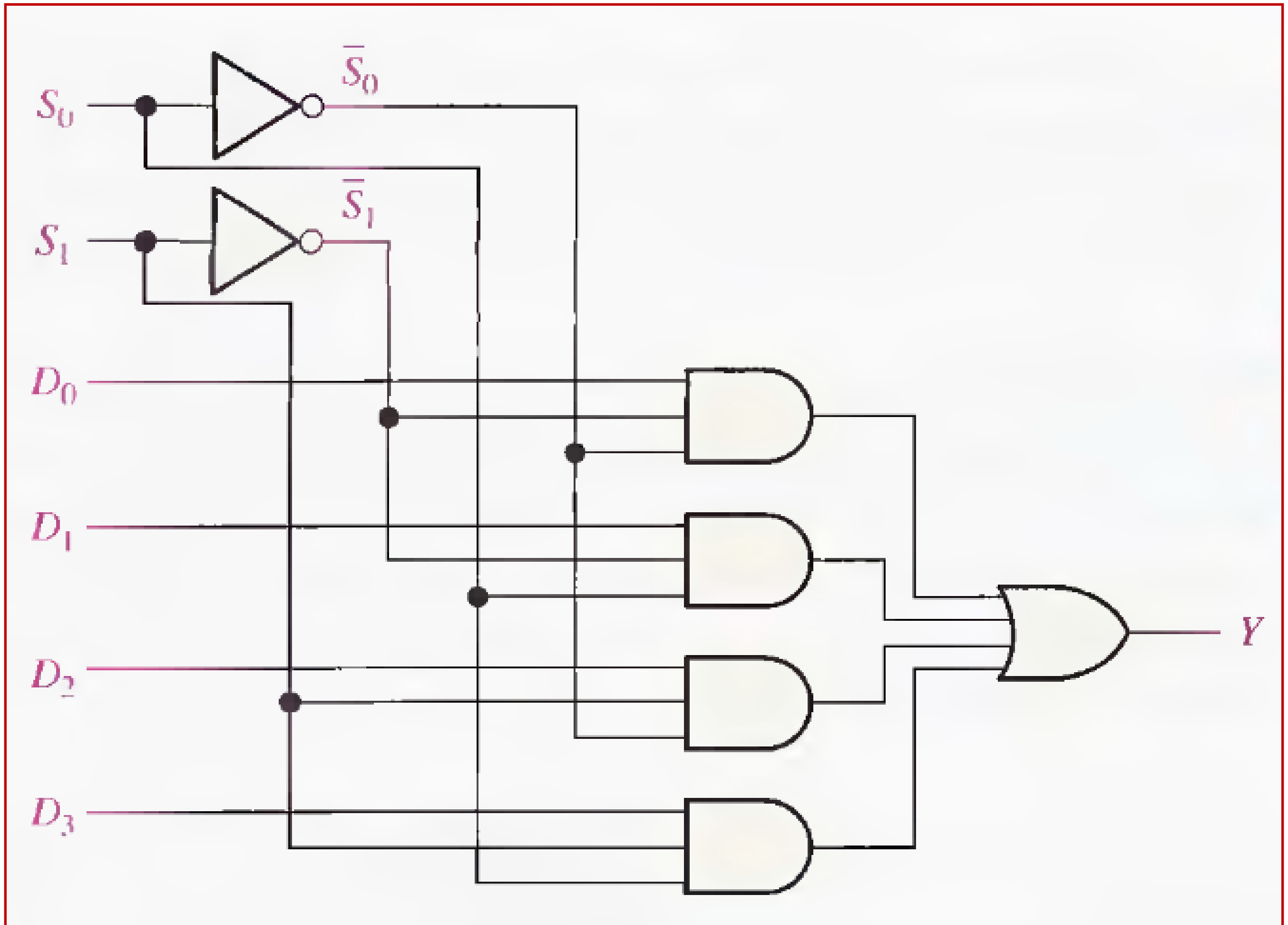
- The data output is equal to the state of the selected data input.
  - You can therefore, derive a logic expression for the output in terms of the data input and the select inputs.

Data output	**S_1**	**S_0**	**Y**
D_0	0	0	$D_0 S'_1 S'_0$
D_1	0	1	$D_1 S'_1 S_0$
D_2	1	0	$D_2 S_1 S'_0$
D_3	1	1	$D_3 S_1 S_0$

$$Y= D_0 S'_1 S'_0 + D_1 S'_1 S_0 + D_2 S_1 S'_0 + D_3 S_1 S_0$$

- The implementation of this equation requires four 3-input AND gates, a 4-input OR gate, and two inverters to generate the complements of S_1 and S_0 .
- Because data can be selected from anyone of the input lines, this circuit is also referred to as a data selector.

Multiplexer

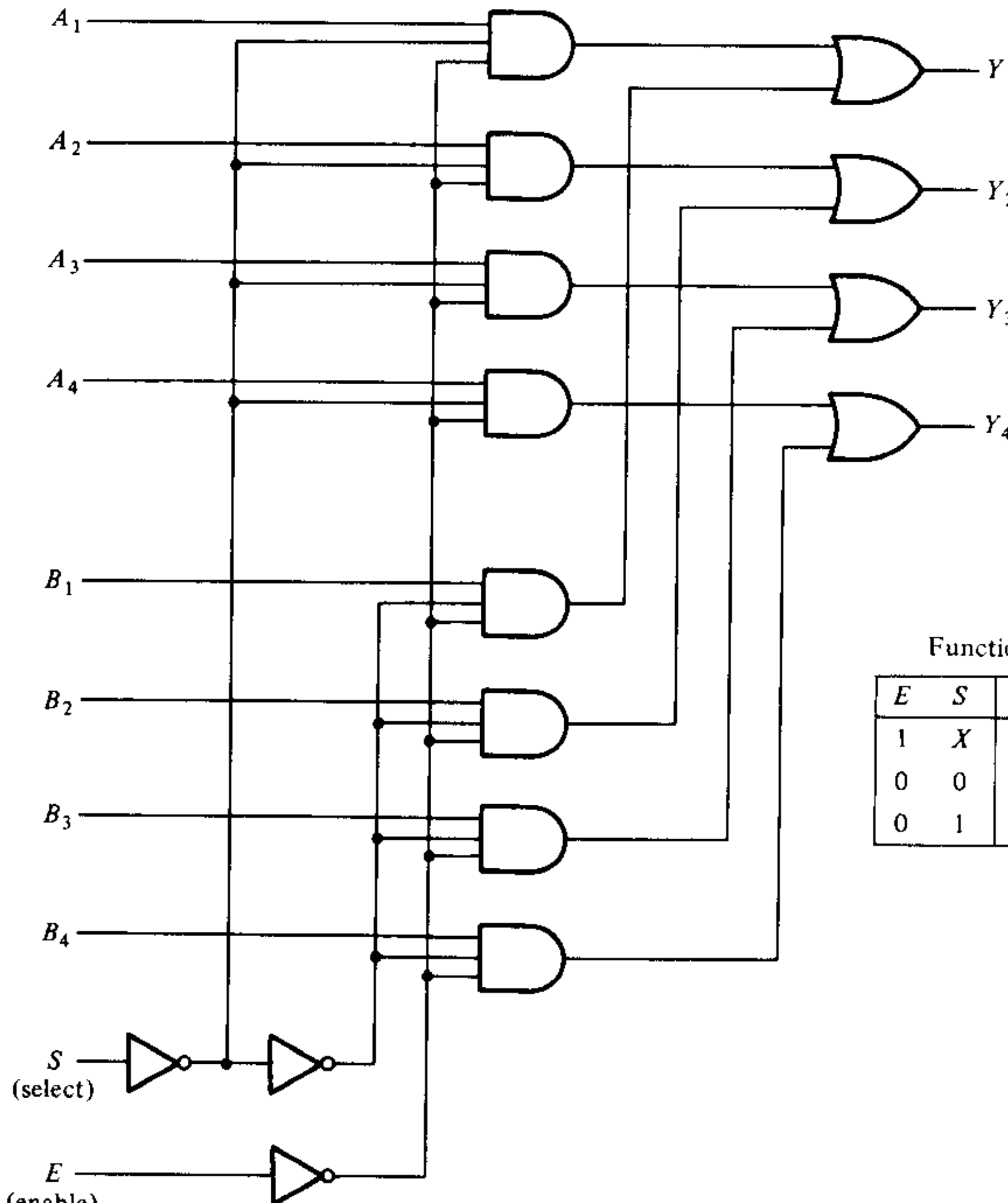


Quadruple

- Two or more multiplexers are enclosed with one IC package.
- The selection and enable inputs in the multiple unit ICs may be common to the multiplexers.
- On the next slide a quadruple 2 line to 1 line multiplexer IC is shown.
- This type of IC is similar to IC type 74157.
- It has 4 MUX, each capable of selecting one of two output lines.

Quadruple

- Output Y1 can be selected to either A1 or B1.
- Output Y2 can be selected to either A2 or B2 and so on.
- One input Selection line S, is enough to select one of two lines in all four multiplexers.
- Enable E is used for activating and deactivating the MUX.
- If S=0, it selects A else B.
- The output have all zero if Enable E=1 regardless the value of the value of S

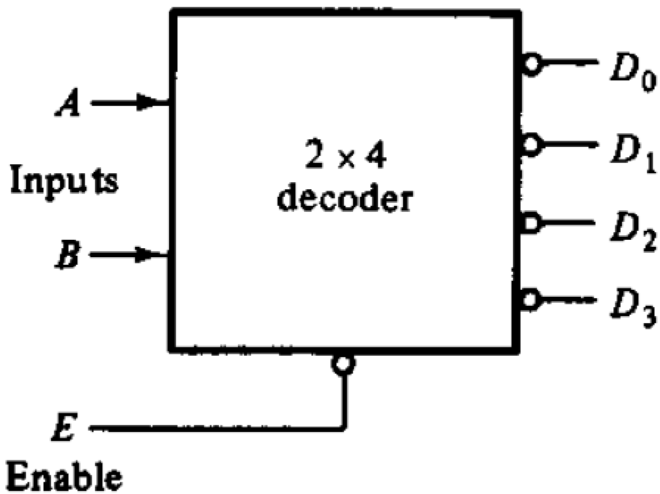


Function table

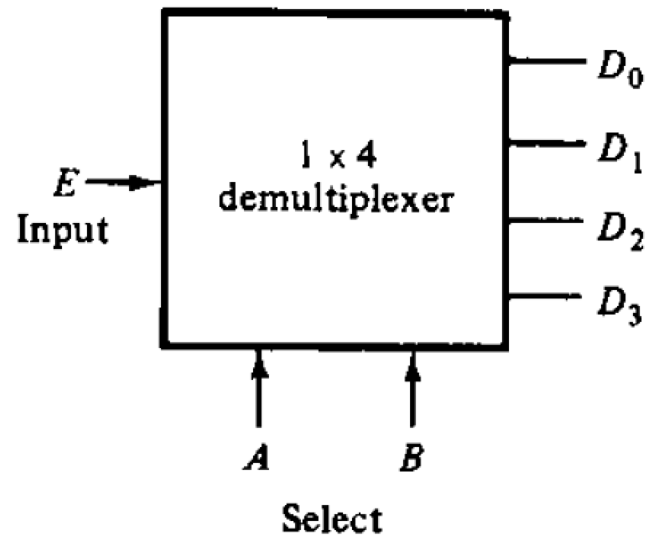
E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B

De-Multiplexer

- Basic functionalities
  - A Demultiplexer (DEMUX) basically reverses the multiplexing function.
  - It takes digital information from one line and distributes it to a given number of output lines.
  - For this reason, the demultiplexer is also known as a data distributor.
  - Decoders can also be used as demultiplexers.

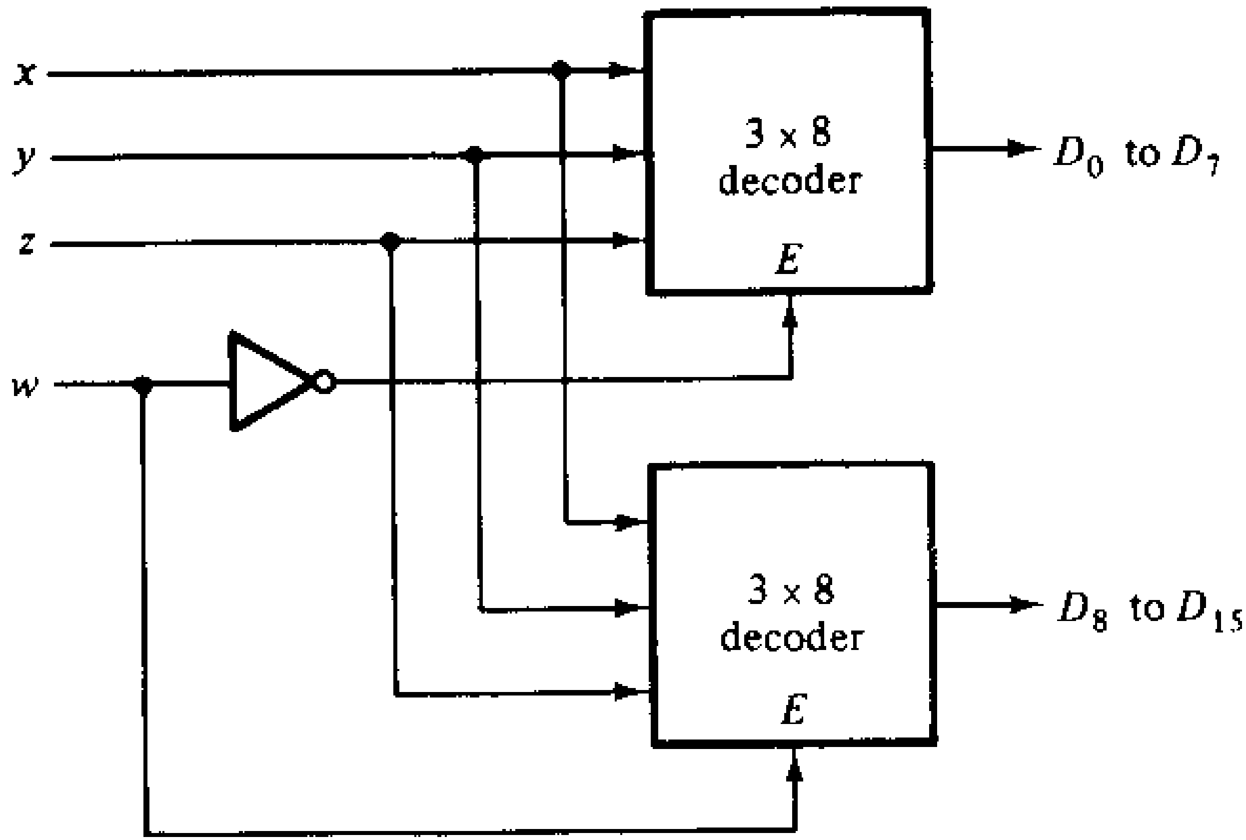


Decoder with Enable



De-Multiplexer

De-Multiplexer

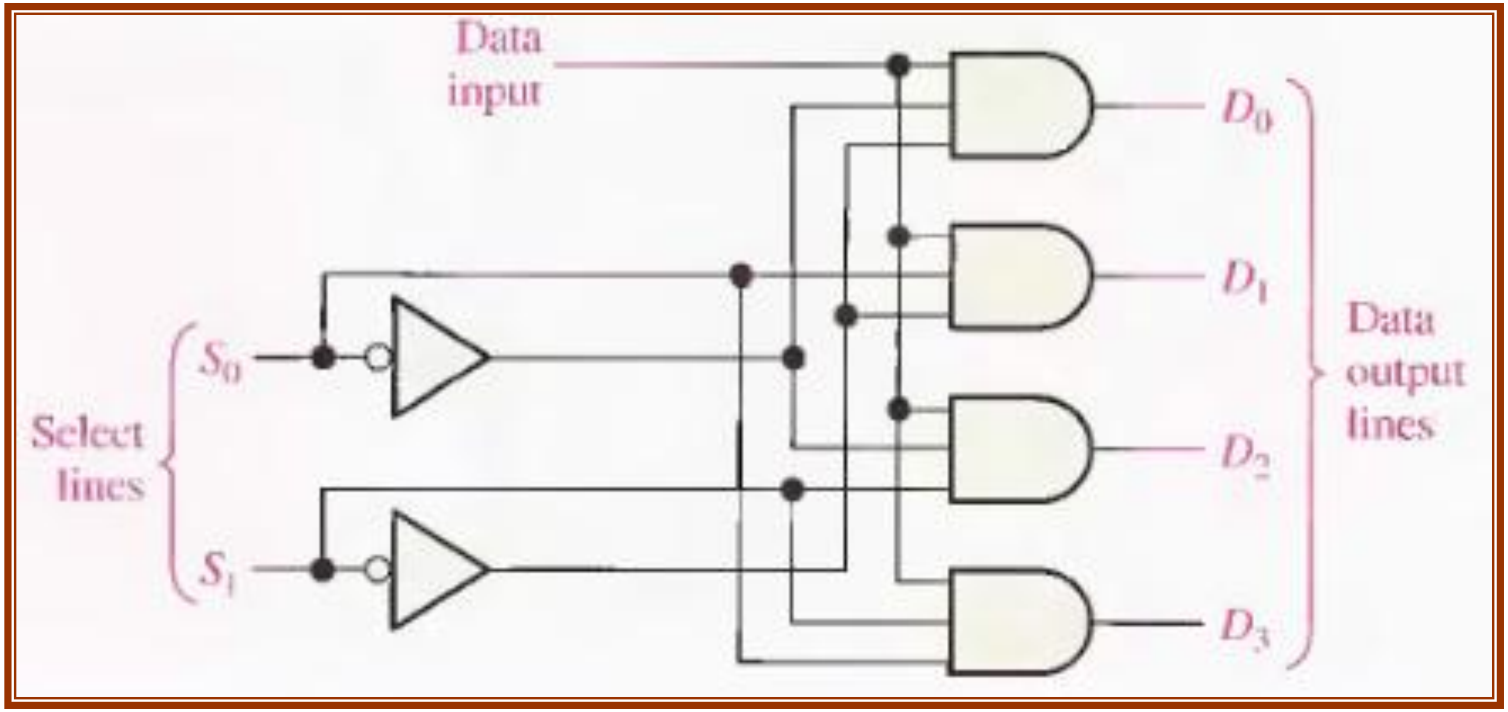


A 4 x 16 decoder constructed with two 3 x 8 line decoders

De-Multiplexer

- Figure on next slide shows 1-line-to-4-line Demultiplexer (DEMUX) circuit.
  - The data-input line goes to all of the AND gates.
  - The two data-select lines enable only one gate at a time, and the data appearing on the data-input line will pass through the selected gate to the associated data-output line.

De-Multiplexer



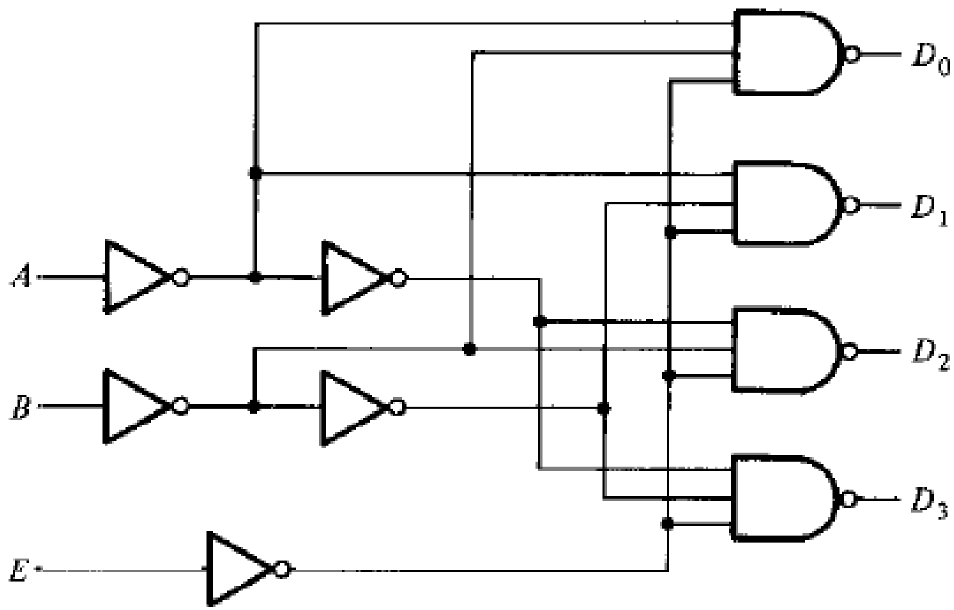
- The De-Multiplexer
  - A decoder with an enable input can function as a demultiplexer.
  - A de multiplexer is a circuit that receives information on a single line and transmit it on to one of 2^n possible output lines.
  - The selection of a specific output line is controlled by the bit values of n selection lines.
  - The decoder can function as a demultiplexer if the E line is taken as data input line and lines A and B are taken as the selection lines.

Procedure

- Figure on slide 4, The data-input line goes to all of the AND gates.
- The two data-select lines enable only one gate at a time, and the data appearing on the data-input line will pass through the selected gate to the associated data-output line.

De-Multiplexer

- The truth table is as



E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Boolean Function Implementation

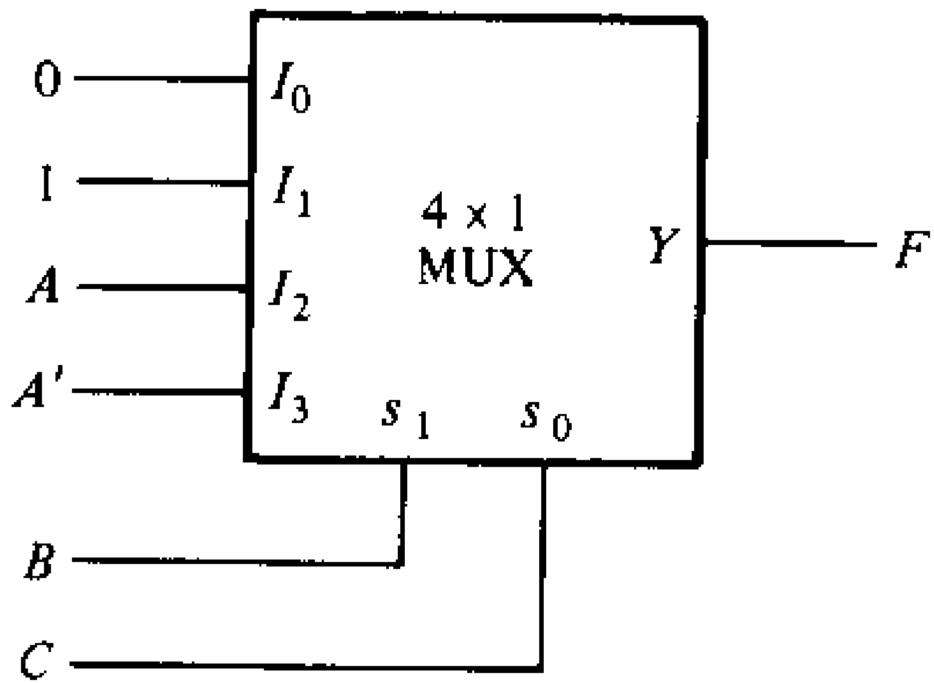
- Decoder can be used to implement a boolean function with addition of one OR Gate.
- In a multiplexer a full decoder with OR gate is present already.
- The minterm out of the decoder to be chosen can be controlled with the input lines.
- Example
  - F(A,B,C)= (1,3,5,6)

Solution

Minterm	A	B	C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

	I_0	I_1	I_2	I_3
A'	0	(1)	2	(3)
A	4	(5)	(6)	7
	0	1	A	A'

Multiplexer implementation



Alternate Solution

- If F(A,B,C) = (1,2,4,5)
- If A and B is selected as Selected input, then

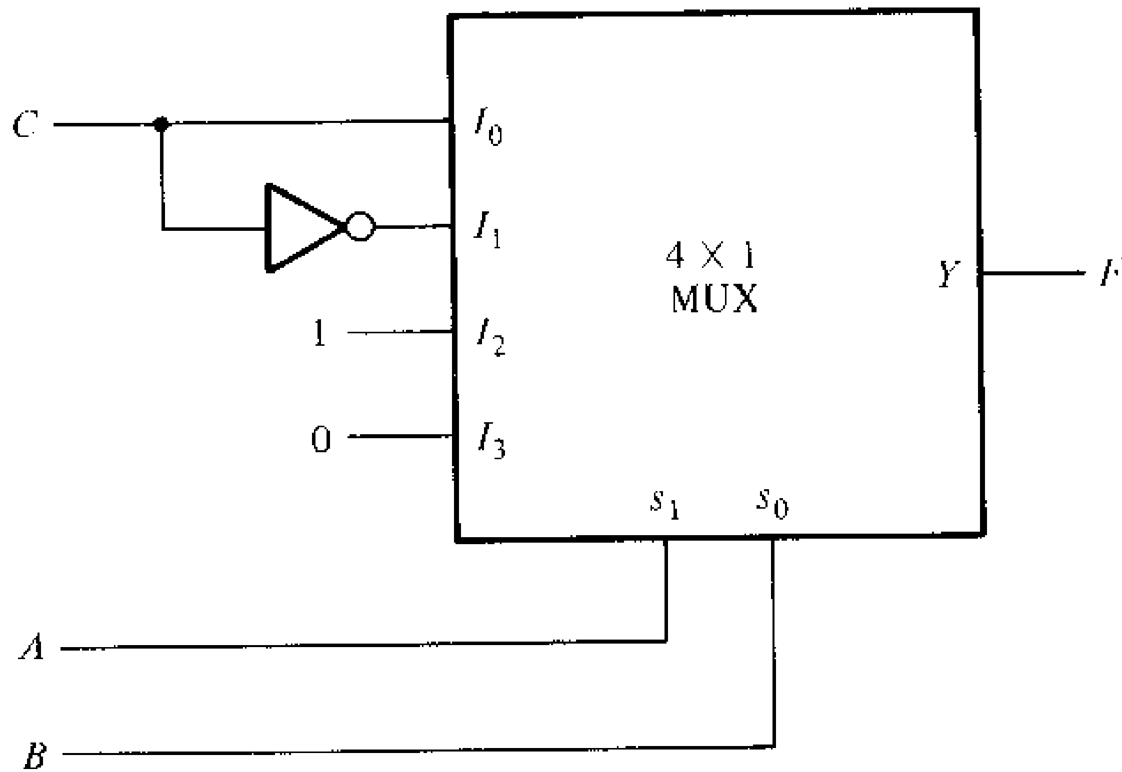
A	B	C	F	
0	0	0	0	$F = C$
0	0	1	1	
0	1	0	1	$F = C'$
0	1	1	0	
1	0	0	1	$F = 1$
1	0	1	1	
1	1	0	0	$F = 0$
1	1	1	0	

(a) Truth table

	I_0	I_1	I_2	I_3
C'	0	(2)	(4)	6
C	(1)	3	(5)	7
	C	C'	1	0

(c) Implementation table

MUX Implementation



Multiplexer connections

Example

Implement the following function with a multiplexer:

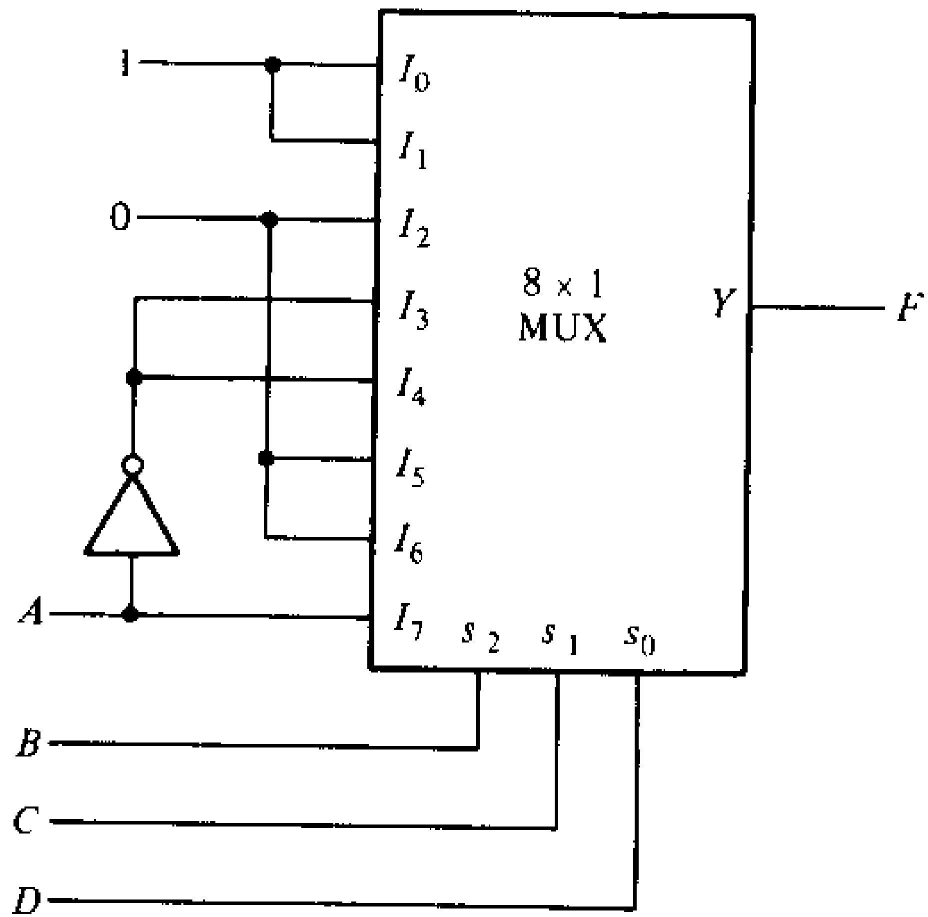
$$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$$

Solution

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	A'	A'	0	0	A

Implementation Table

Solution



Multiplexer connections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