Sequential Logic

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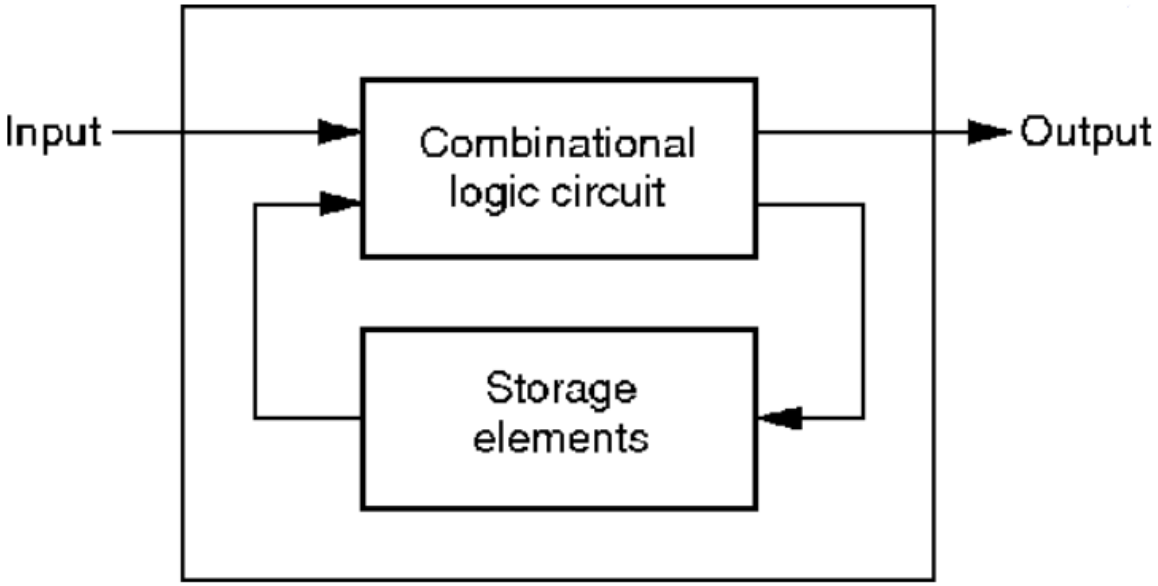
Sequential Logic

- Combinational circuits with memory elements called sequential logic.
- Block diagram of the sequential logic is,



Sequential Logic

- Sequential circuit consists of combinational logic circuit to which memory elements are connected to form a feedback path.
- Memory elements are devices capable of storing binary information within them.
- The binary information stored in the memory elements at any given time defines the state of the sequential circuits.
- For example, ALU Operation, MUX and DeMUX, The Counter Circuits etc

Latches and Flip Flops

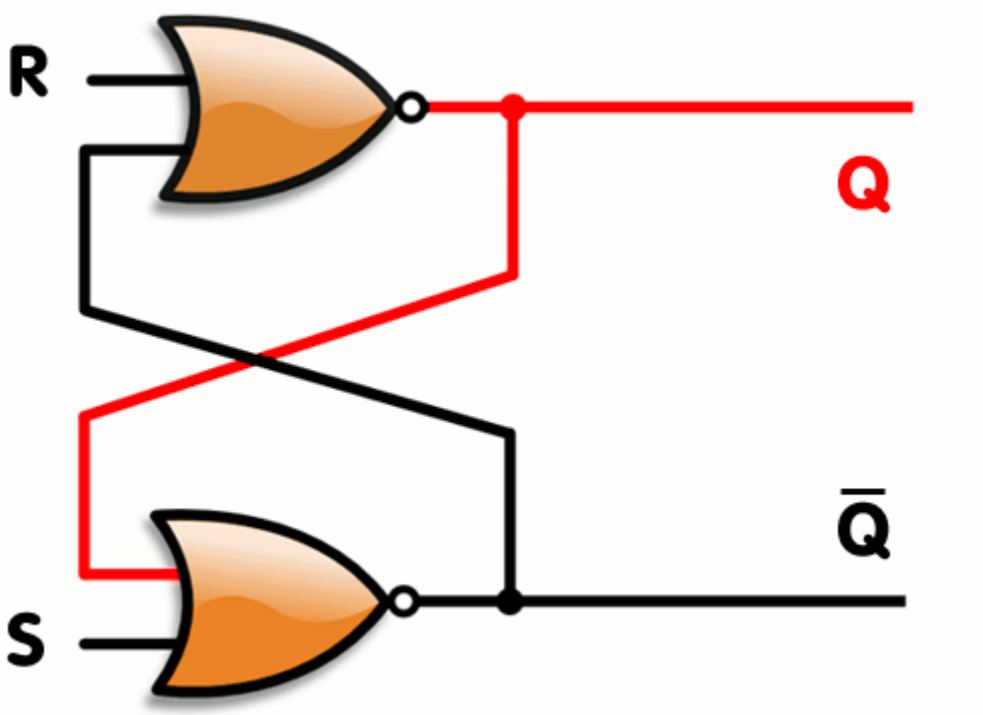
- A latch is a temporary storage device that has two stable states.
- Its output can be changed by applying appropriate inputs.
- A latch normally has two inputs, and two outputs Q and Q'.
- The Latch is said to be in Logic High when,
  - Q=1 and Q'=0
  - And vice versa.

Flip Flops

- A Latch is memory element which is able to retain the information stored in it.
- Flip flop circuit can be constructed from two NAND or NOR Gates.
- The cross coupled connection constitute a feedback.
- Such type of circuits are also called ***direct coupled RS flip flop or SR latch.***

Basic Flip Flop Circuit

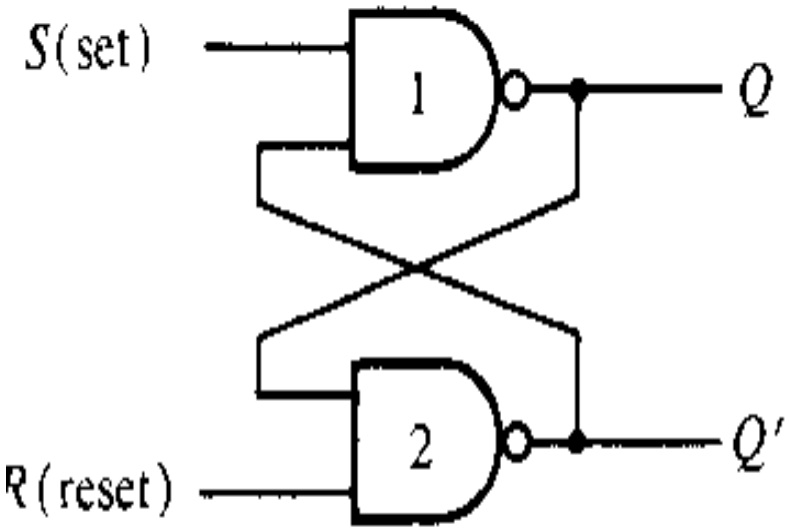
- The figure describes the circuit as follow,



Basic Flip Flop Circuit

- To analyze the operation of the circuits on previous slide,
  - We know that the output of the NOR gate is 0 if any input is one, and vice versa.
  - Starting for the draw run take all the possibilities,
  - Set=1 and Reset=0 then Q=1 and Q'=0
  - Set=0 and Reset=0 then Q=1 and Q'=0 Memory
  - Set=0 and Reset=1 then Q=0 and Q'=1
  - Set=0 and Reset=0 then Q=0 and Q'=1 Memory
  - Set=1 and Reset=1 then Q=0 and Q'=0 (Indeterminate state)

Flip Flop with NAND Gates



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

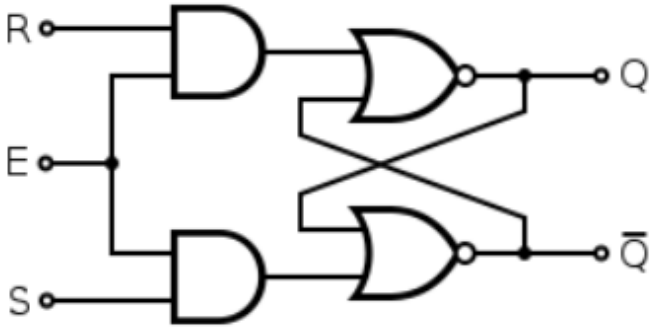
(b) Truth table

For S=1, R=1, Q=0, Q'=1 after S=1, R=0 ➔ Memory
For S=1, R=1, Q=1, Q'=0 after S=0, R=1 ➔ Memory

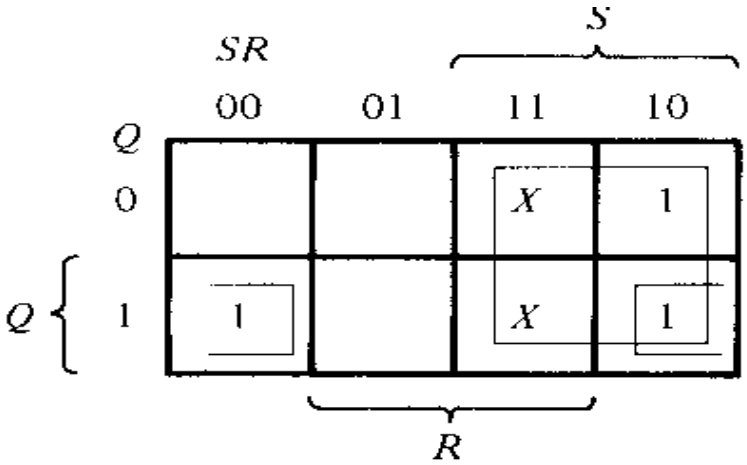
RS-Flip Flop

- The operation of the basic flip flop can be modified by providing an additional control input that determines when the state of the circuit is to be changed.
- An RS flip flop with a clock pulse(CP) is shown.
- It consists of basic flip flop circuit and two additional NAND gates.
- CP acts as an enable signal input.

RS-Flip Flop

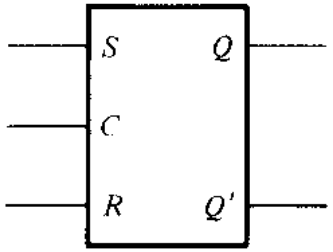


Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Invalid
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	invalid



$$Q(t+1) = S + R'Q$$
$$SR = 0$$

(c) Characteristic equation



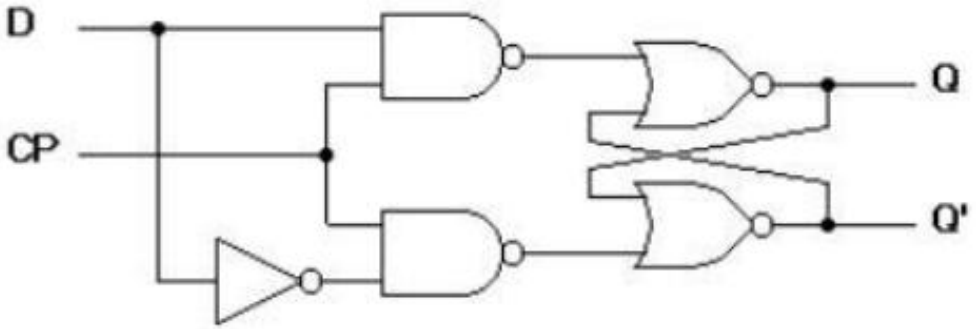
D-Flip Flop

- One way to eliminate the undesirable condition of the indeterminate state in the RS flip flop is to ensure that inputs S and R are never Equal to 1 at the same time.
- It has only two inputs D and CP.
- The D input directly goes to the S input and its complement is applied to R input.
- As long as the pulse input is at 0, the outputs of the gates 3 and 4 are at the one level and the circuit cannot change state regardless of the value of D.

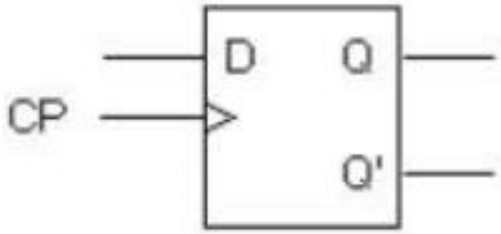
D-Flip Flop

- If D=1,
  - Q output goes to 1, placing the circuit in the set state.
- If D=0,
  - Output Q goes to 0, and circuit switches to the clear state.

D-Flip Flop



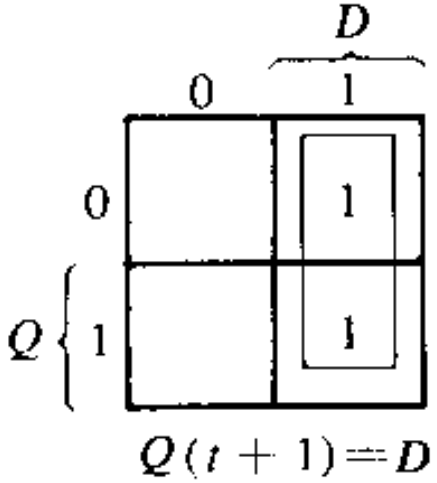
(a) Logic diagram with NAND gates



(b) Graphical symbol

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

(c) Transition table



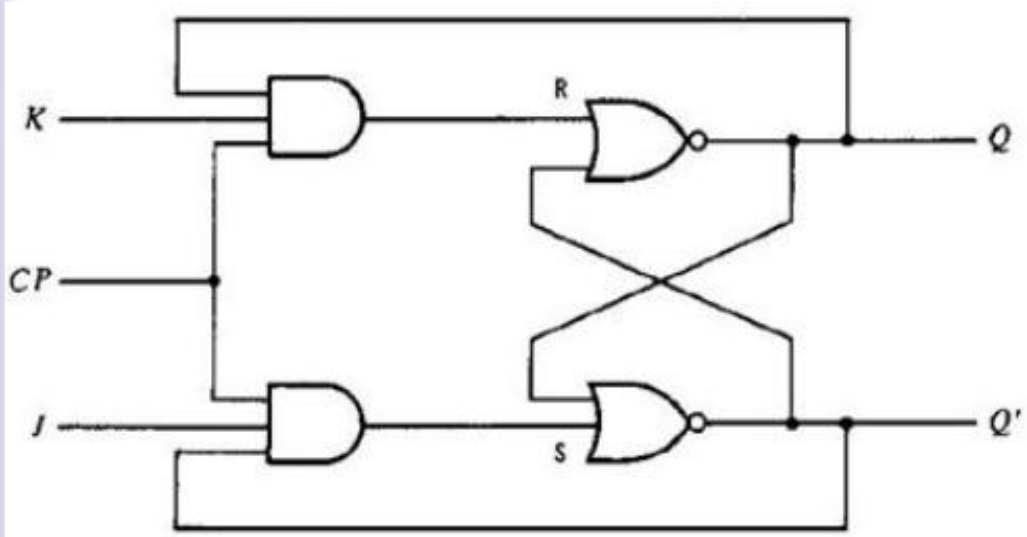
(c) Characteristic equation

JK-Flip Flop

- A JK flip flop is a refinement of the RS flip flop to over come the indeterminate states.
- Input J and K behave like inputs S and R to Set and Clear the flip flop.
- J for Set and K for Reset.
- A JK flip flop is constructed with two cross coupled NOR gates and two AND gates.
- Output Q is ANDed with K and CP inputs
- so that the FF is cleared during a CP only if Q was previously 1.

JK-Flip Flop

- Output Q' is ANDed with J and CP inputs so that FF is set with a CP only when Q' was previously 1.

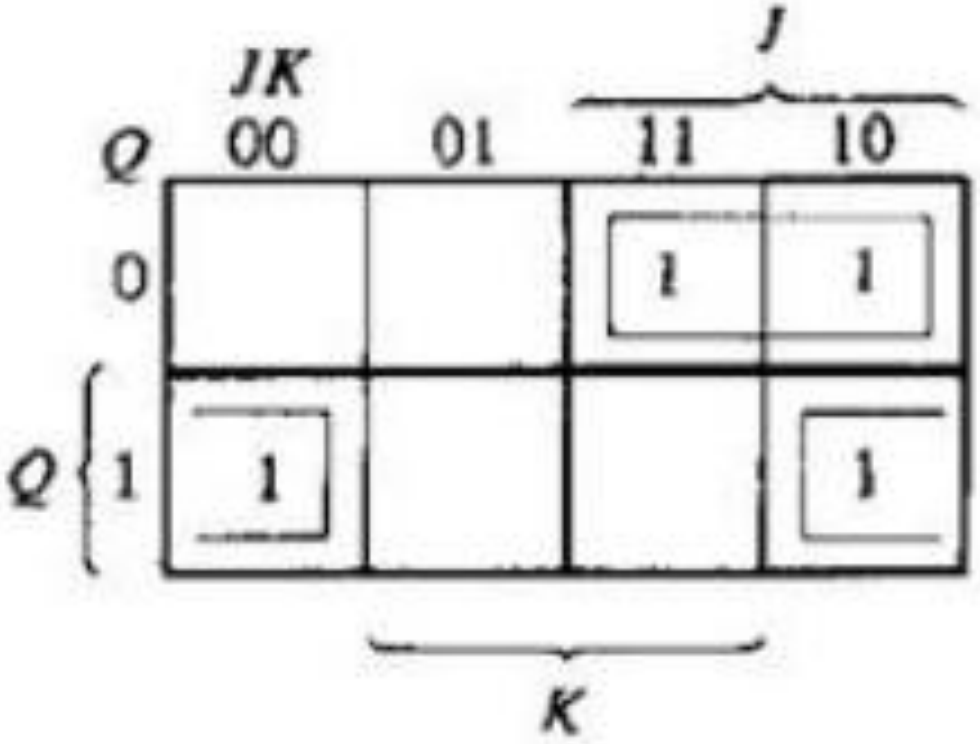


(a) Logic diagram

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Characteristic Table

JK-Flip Flop



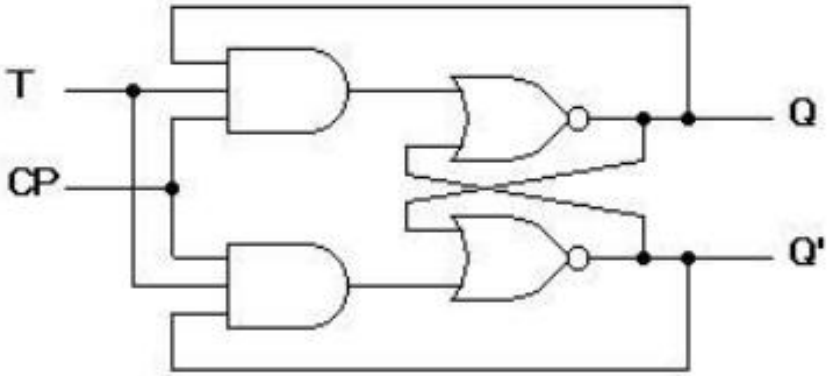
$$Q(t+1) = JQ' + K'Q$$

(c) Characteristic equation

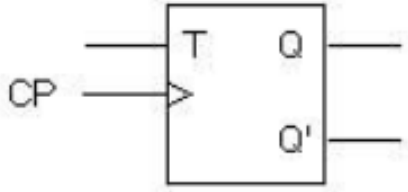
T-Flip Flop

- It's a single input version of JK flip flop.
- The destination T comes from the ability of the FF to "toggle", or complement its state.
- The characteristic table and equation show that when T=0, Q(t+1)=Q, that is, the next state is the same as the present state and no change occurs.
- When T=1, then Q(t+1)=Q' and the state of the FF is complemented.

T-Flip Flop



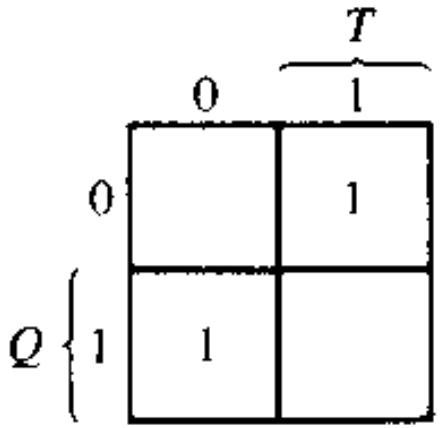
(a) Logic diagram



(b) Graphical symbol

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

(c) Transition table

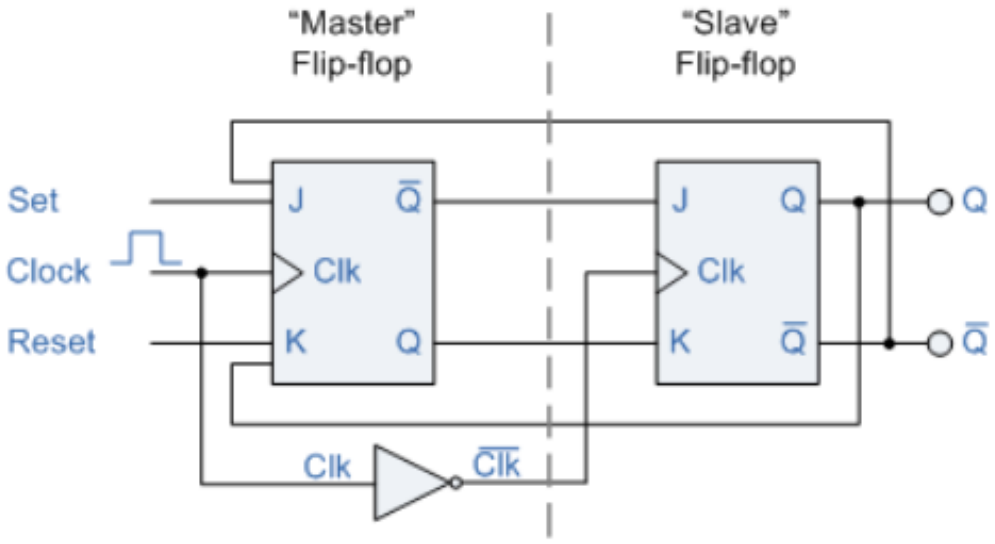


$Q(t+1) = TQ' + T'Q$

(c) Characteristic equation

Master Slave Flip Flop

- A Master Slave FF is constructed from two separate FF.
- One circuit serves as a master and other as a slave, and the overall circuit is called to as a *Master Slave Flip Flop*.



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